REMARKS

Claims 1, 3-4, 6-8, 11, 15-16, 20, 22-23, 25-27, 30 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patents 6,194,928 (HEYNE) 4,255,790 (HONDEGHEM) and 6,100,735 (LU). In response to this rejection, claims 15 and 16 are canceled and claim 17 is rewritten in independent form. The Examiner is respectfully requested to withdraw the rejection of the remaining claims in view of the following arguments distinguishing them over the combination of the cited references.

Claims 1, 3, 4, 20, and 23

The Examiner cites HONDEGHEM as teaching the programmable sequencer element recited in claim 1. While the applicant stands by the rebuttal of this assertion provided responses to previous office actions, the applicant's arguments are rendered mute by LU, since LU's finite state machine (FSM) 34 is just such a programmable sequencer.

With respect to the remaining elements of claim 1, both HEYNE and LU teach an apparatus for generating a pulse sequence employing a first delay stage having some integer number of delay elements (buffers) and a second delay stage having another integer number of delay elements. In each stage, a multiplexer selects the number of delay elements placed in the signal path.

In HEYNE's circuit, the unit delay of one first stage delay element (inverter I1, FIG. 1) and the unit delay of one second stage delay element (inverter I2, FIG. 1) have no relationship to the period of the signal IN being delayed. The delay of an inverter is partly a function of its internal structure, its temperature, and the voltage of its power supply, and HEYNE does not teach that the delays of inverters I1 and I2 should be controlled or adjusted in any way so that they are integer fractions of the period of IN. The Examiner continues to assert that HEYNE teaches that the delays of inverters I1 and I2 are integer fractions of the period of the IN signal, without directly responding to the Applicant's rebuttal to that position. Instead, the Examiner now correctly points to LU as teaching that the delays of delay elements (gates) in LU's circuit (FIG. 3) are integer fractions of the period of the circuit input signal ICLK. The phase detection circuit PD in the first stage 32 of LU's circuit adjusts the delay of each of the M gates in the first stage so that it is $1/M^{th}$ of

the period of the ICLK signal. Thus assuming that ICLK has a period of Tp, the first stage 32 can adjust delay with a resolution of T/M. The "first means" of the applicant's claim 1 therefore reads on LU's first stage 32 because stage 32.

a. generates a "second pulse sequence" (K) in response to a "first pulse sequence" (ICLK)

b. with a first delay adjusted by first control data (MSB's)

c. with a resolution of Tp/N (where N is the number of delay elements in stage 32)

d. over a first range substantially wider than Tp/M (since the range of stage 32 is exactly Tp).

In LU's second stage 30, the phase detection circuit 36 adjusts the delay of each delay element to be $1/P^{th}$ of the delay Tp/N of the first stage element, where P is the number of delay elements in the second stage. Thus the resolution of the second stage 30 is Tp/(N*P), which we can consider to be Tp/M if we define M as M = N*P. Thus, the following limitations of the applicant's "second means" also read on LU's second stage 30:

a. it generates a "third pulse sequence" (CLK_OUT) in response to the "second pulse sequence" (K)

b. with a second delay adjusted by second control data (LSB's), and

c. with a resolution of Tp/M.

However, the "second means" of the applicant's claim 1 does not fully read on LU's second stage 30. Since the range over which LU's second stage 30 is able to adjust its delay is exactly Tp/N, unlike the applicant's recited "second means", LU's second stage 30 does not adjust the second delay over a second range substantially wider than Tp/N as recited in claim 1. LU directly teaches that the range of second stage 30 should be exactly Tp/N, and it would not be obvious for one of skill in the art to modify LU's circuit so that stage 30 would have a range substantially (or even slightly) wider than Tp/N because LU provides no motivation for doing so. LU teaches that first delay stage 32 provides a gross delay with a resolution of Tp/N and that second delay stage 30 provides a fine delay with a resolution of Tp/(N*P). In the context of LU's teaching, given that the second

stage 30 is to provide a set of fine delay adjustment steps between the gross adjustment steps of Tp/N provided by first stage 32, giving stage 30 a range wider than Tp/N would serve no useful purpose. Although the applicant does teach a very good reason for providing a second delay stage having a much wider range than Tp/N (i.e. it helps the circuit produce surprisingly high overall resolution, much higher than LU's circuit, when M and N are relatively prime), such motivation is not found in the teachings of LU or any other cited reference.

Thus, the applicant concedes that LU alone discloses every limitation of the applicant's claim 1 except one, that the delay range of the second means is "substantially wider than Tp/N". Since it would not be obvious or even beneficial to make the range of the LU's second stage 30 any wider than Tp/N, and since none of the cited references motivates one of skill in the art to provide LU's second stage with a range wider than Tp/N, the applicant's claim 1 is patentable over the cited combination of references.

Claims 3, 4, 20, and 22 are patentable over the combination of the cited references for reasons expressed above in connection with claim 1.

Claim 23

During initialization of HEYNE's circuit, the IN signal is made periodic, and HEYNE adjusts the total delay of the circuit to as nearly phase align the IN and OUT signals as possible given the resolution of the delay circuit. Thus the total range of HEYNE's delay circuit must be somewhat larger than the period of the IN signal (which we call Tp) during initialization. HEYNE teaches to use stage 2 to grossly adjust the delay and to use stage 1 to finely adjust the delay. The reason there are two stages in HEYNE (and also in LU) is because using a gross adjustment stage and a fine adjustment stage, instead of just a single stage, greatly reduces the number of delay elements needed to provide both the desired range and resolution.

In order for HEYNE's delay circuit to work, the gross adjustment stage 2 should have a range at least a little larger than the expected value of Tp. The range of gross adjustment stage 2 is therefore M*t2 > Tp, where M is the number of elements I2 in the stage and t2 is the unit delay of elements I2. Thus, t2 should be at least Tp/M. To provide fine adjustment of delay, the range N * t1 of stage 1 (where N

is the number of elements t1 in stage 1 and t1 is the unit delay of each element I1) need be not much larger than t2 = Tp/M.

In the advisory action, the Examiner's assertion that the range of stage 1 must be Tp in order for the circuit to function properly after initialization is unwarranted. HEYNE teaches that once the delay is initialized by selecting some number of elements I1 and I2 in the IN-to-OUT signal path so that the total delay is as nearly as possible Tp, within the resolution of the delay circuit, it is necessary to thereafter adjust the number of fine delay elements I1 in the signal path to compensate for changes in delay due to temperature variations. Thus, the range of stage 1 need only be a fraction of Tp since the temperature variations are only going to make the delay vary by a fraction of the set point delay Tp. HEYNE (col. 5, lines 49-55) tells us that the range of stage 1 need be at least 3*t2. However, one of skill in the art would not be motivated to make the range of stage 1 at least as large as Tp since doing so would require stage 1 to include an excessively large number of inverters I1 and would render stage 2 superfluous, since stage 1 alone would have the both the required range and resolution.

Note that in the applicant's circuit, both the stages are gross adjustment stages, in the sense that neither stage alone has the desired resolution, and both stages have the range Tp.

Claims 6 and 25

Claims 6 and 25 recite that the "third pulse sequence is periodic". The applicant stipulates that the OUT signal of HEYNE and the CLK_OUT signal of LU can be periodic, however claims 6 and 25 are patentable over the cited references for reasons discussed above in connection with their parent claims 1 and 20.

Claims 7 and 26

The Examiner incorrectly cites HEYNE as teaching the additional limitations of claim 7, since as described above in connection with claim 4, the delays t1 and t2 provided by HEYNE's inverters are selected as functions of the maximum range in fluctuation of overall circuit delay due to temperature changes. However, the applicants stipulate that LU teaches the additional limitations of claims 7 and 26. Claims 7 and 26 are nonetheless patentable over the cited

references for reasons discussed above in connection with their parent claims 1 and 20.

Claims 8 and 27

The Examiner incorrectly cites HEYNE as teaching that the delays of gates of either of the HEYNE's delay stages is Tp/M where Tp is the period of the input signal and M is an integer, since as described above in connection with claim 4, the delays t1 and t2 provided by HEYNE's inverters are selected as functions of the maximum range in fluctuation of overall circuit delay due to temperature. However, the applicant stipulates that LU teaches the additional limitations of claims 8 and 27. Claims 8 and 27 are nonetheless patentable over the cited references for reasons discussed above in connection with their parent claims 1. and 20.

Claims 11 and 30

The Examiner incorrectly cites HEYNE as teaching the additional limitations of claims 11 and 30, since as described above in connection with claim 4, the delays t1 and t2 provided by HEYNE's inverters are selected as functions of the maximum range in fluctuation of overall circuit delay due to temperature. However, the applicant stipulates that LU teaches the additional limitations of claims 11 and 30. Claims 11 and 30 are nonetheless patentable over the cited references for reasons discussed above in connection with its parent claims 1 and 20.

Claims 15 and 16

The Examiner incorrectly cites HEYNE as teaching the additional limitations of claim 15, since as described above in connection with claim 4, the delays t1 and t2 provided by HEYNE's inverters are selected as functions of the maximum range in fluctuation of overall circuit delay due to temperature and are not functions of the period of the input signal. However, claims 15 and 16 are canceled in view of LU.

Claims 34 and 35

Claims 34 and 35 recite that M and N are relatively prime, and the Examiner has indicated at paragraph 22 that the cited references

HEYNE, LU and HONDEGHEM do not teach this. The Examiner has rejected various other claims reciting that M and N are relatively prime in view of the combination of HEYNE, LU, HONDEGHEM and LIEDBERG (U.S. Patent 5,471,165), since the Examiner is under the impression that LIEDBERG teaches M and N are relatively prime. However, the Examiner has not applied LIEDBERG against 34 and 35. Claims 34 and 35 are patentable over the combination of the HEYNE, LU, HONDEGHEM and LIEDBERG for reasons set forth below in connection with claims 2, 5, 21 and 24.

2. The Examiner rejects claims 9-10, 12-14, 17-19, 28-29, 31-33 and 36-38 under 35 U.S.C. 103(a) as being unpatentable over the combination of HEYNE, LU, HONDEGHEM and LIEDBERG (U.S. Patent 5,471,165). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following remarks distinguishing these claims over the cited references.

Claims 9, 10, 12-14, 17-19, 28, 29, 31-33, 36-38

The applicant's FIG. 5 shows a delay circuit having two stages 54 and 56, the "first and second means" of claim 1. Stage 54 delays pulses of a clock signal ROSC to produce pulses of an output CLOCK signal, and stage 56 further delays pulses of the CLOCK signal to produce pulses of a CLOCK' signal. Claim 9 recites the architecture for the "second means" as detailed by the applicant's FIG. 7

It is helpful in understanding claim 9 to compare LU's second stage architecture (blocks 30 and 28, FIG. 3) to the applicant's second stage architecture (FIG. 7). LU's second stage has two inputs, the Kth and (K+1) the taps of delay line 32 as selected by multiplexers 26. We assume ICLK has a period of Tp. Since the delay elements of delay line 32 have delays of Tp/M, where M is the number of delay elements of delay line 32, edges of the selected Kth and (K+)the taps of delay line 32 arrive at delay line 30 Tp/N seconds apart. Control circuit 36 adjusts the delay of the delay elements of delay line 30 so that each has a delay of 1/P of the period between the Kth and (K+1)the tap signals, where P is the number of delay elements in delay line 30. Thus, the delay of each element of delay line 30 is Tp/(M*P). If we let N = M*P, then the delay of each element of delay line 30 is Tp/(M*P). The unit delay of each of LU's

second stage elements is an integer fraction P of the unit delay of each of LU's first stage delay elements. As discussed above, it is impossible to choose values of M, N and P for which M and N are relatively prime since N = M*P, and P is an necessarily an integer.

The applicant's first stage circuit of FIG. 8, uses N delay elements, each adjusted by PL controller 106 to provide a delay that its 1/Mth the period of the ROSC signal. The applicant's second stage circuit of FIG. 7 uses delay elements 60 to delay the CLOCK signal to produce the CLOCK' signal, but the unit delay of each delay element of the second stage is not an integer fraction of the unit delay of each element of the first delay stage as taught by LU. The unit delay of each element 60 of FIG. 7 is controlled by controller 70 so that it is 1/Mth of the period of the ROSC signal, where M is the number of gates 66 in the feedback path between the inputs of controller 70. Since M and N are independently selectable integers in the applicant's circuit, they can and are made relatively prime.

Claim 9 reads on the architecture of the applicant's FIG. 7. The "second gates" are gates 60, and the third gates are gates 66. LU does not teach this delay circuit architecture, since LU does not teach the recited third gates.

The Examiner cites LIEDBERG's gates D1 as being the "second" gates of claim 9 and gates D2 as being the "third gates" of claim 9. However, if D1 are the second gates, then we must consider signal SO to be the recited "second pulse sequence" and must consider signal S1 to be the recited "third pulse sequence". LIEDBERG's FIG. 3 therefore shows gates D2 as receiving the "third pulse sequence" as input rather than the "first pulse sequence" as recited in claim 9. Note in the applicant's FIG. 7 that the "third gates" 66 do not receive the se output signal of the second gates 60. It receives the same input signal (ROSC) as the "first gates" 104 of FIG. 8. It is not enough for the Examiner to point out that LIEDBERG has two sets of gates with the same delays. To show that LIEDBERG anticipates the limitations of claim 9, the Examiner must show that LIEDBERG advocates interconnecting them in the manner recited in claim 9. LIEDBERG does not do that.

Claims 9, 10, 12-14, 17-19, 28, 29, 31-33, 36-38 are patentable over the cited references for similar reasons.

3. Claims 2, 5, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over HEYNE, LU and HONDEGHEM in view of U.S. Patent 5,838,753 (GORBICS). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following remarks distinguishing them over the cited prior art.

Claims 2, 5, 21 and 24

LU and HEYNE advocate using a two-stage delay circuit including a gross adjustment stage having a wide range but a low resolution, and including a fine adjustment stage having a narrow range but high resolution. The combination of the two stages provides a wide range and high resolution delay adjustment using far fewer delay elements than a single stage having the same range and resolution.

The applicant's invention as recited in claim 2 is to use two gross adjustment stages in which both stages have relatively wide ranges and relatively low resolutions. However, in the applicant's circuit M and N (the ratios of their resolutions to the period of their input signal) are made relatively prime because doing so provides an overall resolution for both stages that is (surprisingly) very much greater than the resolution of either stage alone. For a given range and resolution, the applicant's two-stage delay circuit requires substantially fewer delay elements than HEYNE's or LU's delay circuits.

Accordingly, parent claim 1 recites that the resolutions of the first and second means are Tp/M and TP/N where M and N are integers, and claim 2 further recites that integers M and N are relatively prime. As discussed in the applicant's previous responses, the resolutions of the first and second stages of HEYNE's circuit are independent of the period of the circuit input signal and are therefore not Tp/M and Tp/N. LU does teach that the delay resolution of first stage 32 is Tp/M, if we assume the period of ICLK is Tp and that the number of buffers in stage 32 is M. The resolution of the second stage 30 is Tp/(M*P) if we assume there are P buffers in second stage 30. Defining N as N= M*P, the resolution of second stage 30 is Tp/N.

Clearly in LU's circuit, M and N are not relatively prime since N is necessarily an integer multiple P of M. The Examiner no longer relies on HEYNE as teaching that M and N are relatively prime, and

correctly determines that LU does not teach M and N are relatively prime, but now relies on newly cited GORBICS as teaching this, and that in view of GORBICS it would be obvious to modify LU to render M and N in LU's circuit relatively prime.

In order to show that the additional limitation claim 2 would be an obvious modification to LU, GORBICS should at minimum motivate one of skill in the art to modify LU's circuit in some way to make those particular parameters M and N of LU relatively prime. However making such a modification would not be a simple matter of adjusting the numbers M and P of buffers in LU's first and second stages so that M and N are relatively prime. Since LU's architecture requires that N = M*P, and that N, M and P all be integers, there are no possible combinations of integer values of M, N and P for which M and N are relatively prime. Thus regardless of how much GORBICS might motivate one of skill in the art to adapt LU to provide values of M and N that are relatively prime, it would not be possible to make M and N of LU's circuit relatively prime simply by adjusting the numbers M and P of buffers in the delay stages 32 and 30. It would be necessary to substantially modify LU's architecture in a way that renders N something other than an integer multiple of M. Thus it would be necessary for GORBICS to not only motivate one of skill in the art to make M and N relatively prime, but also necessary for GORBICS to provide some indication as to how that might be done, since the architecture of LU's circuit would have to be substantially altered.

GORBICS (FIG. 2) shows a device for measuring a time interval between edges of input signal t_{event}. A counter 30 counts the number of whole cycles of a CLOCK signal occurring between edges of t_{event} and an interpolator 32 determines any additional fraction of a clock cycle, and realignment circuit 34 adds the two values to produce a measured output. The Examiner points to GORBICS col. 4, lines 19-50 as teaching that there are parameters N and H associated with the circuit of FIG. 2 that are relatively prime and that GORBICS' parameters N and H are equivalent to the applicant's parameters M and N.

The cited column 4, lines 19-50 talk about GORBICS' FIG. 3 (the interpolator 32 of FIG. 2), rather than about the timing measurement device of FIG. 2. Interpolator 32 of FIG. 3 includes a delay circuit 40 in which a phase locking circuit (not shown) controls the switching

delay of each of its buffers 40_0 to 40_{n-1} so that it has a unit delay of (T*H)/N, where

T is the period of the CLOCK signal,
N is an integer number of delay elements in circuit 40, and
H is an integer harmonic number.

Col. 4, lines 38- 45 gives the example that when N = 16, H = 3 and T is 3.2 ns, then the delay (T*H)/N of each buffer is (3.2 ns*3)/16 = 600 ps. Thus, the resolution of delay circuit 40 is T/(N/H). If we assume that M=N/H, then the resolution of delay circuit 40 is T/M which is similar in form to that recited for the first means of the applicant's parent claim 1. In the example provided by GORBICS,

M = N/H = 16/3 = 5.333

which is clearly not an integer as recited in claim 1.

Claim 2 further recites that the values of M and N of parent claim 1 are relatively prime. Parent claim 1 defines M as the ratio of clock period Tp to resolution of the "first means" and defines N is the ratio of clock period TP to resolution of the "second" means of claim 1. Parent claim 1 also recites that M and N are integers. Since GORBICS teaches that GORBICS' N and H parameters should be relatively prime (col. 4, lines 31-33) and that the ratio (M) of clock period to unit delay resolution) should be N/H, then for GORBIC's delay circuit 40, the value of ratio M will always be other than an integer as recited in the parent claim 1 of claim 2. Thus the effect of GORBICS, to the extent it might be applied to LU, is not to teach the limitations of claim 2, but to teach away from limitations of parent claim 1. Where LU teaches to make delay resolutions of both stages integer fractions of the clock period as recited in claim 1, GORBICS teaches to make a delay resolution a non-integer fraction of a clock period. Thus GORBICS' teachings do not motivate one of skill in the art to make LU's circuit more like the apparatus of claim 2; they may motivate one to make it less like the apparatus of parent claim 1.

It should be understood that claim 2 recites each of the two parameters M and N claim 2 recites as being relatively prime is a ratio between a clock period Tp and a delay resolution of a separate delay stage. Neither of the two relatively prime parameters of GORBICS' circuit is such a ratio. GORBICS' H parameter is a harmonic number, and GORBICS' N parameter is a ratio of the period of a higher harmonic (T*H) of the clock signal to stage delay resolution . Thus while the Examiner correctly observes that GORBICS' two parameters N and H that are relatively prime, those two parameters are not the same kind of parameters as the M and N parameters recited in claims 1 and 2. That is why the teaching of GORBICS, when applied to LU, make LU's circuit less like the apparatus of claims 1 and 2.

Claims 5, 21, 24, 34 and 35 are patentable over the cited references for similar reasons.

In view of the foregoing amendments and remarks, it is believed that application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
16100 N.W. Cornell Road, Suite 220
Beaverton, Oregon 97006

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: CRED 2164

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Penelope Stockwell

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